Study And Characterisation Of Electrolytic Capacitor-Bank And Ultra Capacitor Energy Source In DSTATCOM

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Abstract-**This paper discusses the dynamic performance and the modeling of a DSTATCOM with Capacitor Bank (CB) and Ultra Capacitor Energy Storage (UCES) considering their equivalent series resistance for improving the operation of power quality in power distribution system. The proposed integrated DSTATCOM system is studied for riding through voltage sags and dynamically controlling active power independently of reactive power for stability augmentation purposes. Simulation is done using Sim Power Systems of MATLAB/Simulink to validate the proposed global system. The simulation results show that the DSTATCOM has superior performance with ultra capacitor over capacitor-bank (electrolytic type).**

1 INTRODUCTION

Recently, with the growth of industry manufacturers and population, electric power quality becomes more and more important. As one of the most power quality issues such as flicker due to feeder voltage fluctuation, influencing domestic lighting and sensitive apparatus of nearby transmission and distribution system. Electric arc furnace (EAF), as a major industry customer of supply utility, consumes considerable real power and reactive power with the time-varying, stochastic and even chaotic characteristics during melting and refining process, and therefore generates severe flicker to the grid. During the switching on and off of these loads, the demanded high currents determine a voltage drop across the line impedance which is responsible for voltage fluctuations. Voltage fluctuation causes an annoying variation in the output illumination from incandescent or fluorescent lamps. The severity of the annoyance is generally dependent on the frequency and amplitude of the voltage variation and the short circuit capacity of the PCC (point of common coupling). [1]

2 POSSIBLE SOLUTIONS OF POWER QUALITY PROBLEMS

There are many solutions in mitigating the power quality problems at a distribution system such as using surge arresters, active power filters, isolation transformer, uninterruptible power supply, and static VAR compensator. A group of controllers together called Custom Power Devices (CPD), which include the DSTATCOM (distribution static compensator), DVR (dynamic voltage restorer) and UPQC (unified power quality conditioner) are used for compensating the power quality problems in the current, voltage and both current and voltage respectively in very short time. DSTATCOM is a shunt-connected device. It takes care of power quality problems in the currents.[11]

3 DSTATCOM

FACTS-based power electronic controllers for electric distribution systems, namely custom power (CP) devices, are able to enhance the reliability and quality of power provided to customers. A DSTATCOM is a fast response, solid-state power controller that provides flexible voltage control at the point of connection (PCC) to the utility distribution feeder for power quality (PQ) improvements. It can continuously generate reactive power by varying the amplitude of the inverter voltage with respect to the line bus voltage so that a controlled current flows through the tie reactance between the DSTATCOM and the distribution network takes place.

3.1 Features of DSTATCOM:- The DSTATCOM mitigate voltage fluctuations such as sags, swells, transients to provide voltage regulation, power factor correction and harmonics compensation.[2]

3.2 DSTATCOM With DC Sources:- DSTATCOM can exchange both active and reactive power with the distribution system by varying the amplitude and phase angle of the converter voltage with respect to the line terminal voltage, if an energy storage system (ESS) is included into the dc bus. As a result a controlled current flow through the tie reactance between the DSTATCOM and the distribution network. This enables the DSTATCOM to mitigate voltage fluctuations and to correct the power factor of weak distribution systems in instantaneous real-time. In the figure 3,the VDC is DC source. There are two types of DC sources

3.2.1 Battery energy storage system (BESS):-In battery energy storage system lead acid batteries are mostly used because lead acid batteries offer a more economical solution for application in the mitigation of flicker that require small devices for supplying power for small period of time and intermittently. The energy stored in a lead acid battery is chemical energy that is translated into electrical energy. Lead acid batteries are rechargeable.[1]

3.2.2 Capacitor bank. Capacitor bank is of two types,

Limitations with BESS	Limitation with ECB	Advantages with UCES
Low power density.	Low power density.	High power density.
It required proper maintenance, low reliability.	More reliable than BESS.	No maintenance, high reliability.
Small change in temperature effect the performance.	Low over and under temperature capacity.	Wider operating temperature range.
It affected by the ageing effect.	Ageing effect also affects the ECB.	No ageing effect upto 5 to 10 years.
Limited life.	Life up to 100,000 cycles.	Low degradation after 100,000 cycles.
Charge/recharge capability is very slow.	Charge/recharge capability is more than BESS.	Rapid charge/recharge capability within seconds.

3.2.2.a) Electrolytic type capacitor bank (ECB):-An aluminum electrolytic capacitor consists of cathode aluminum foil, capacitor paper (electrolytic paper), electrolyte, and an aluminum oxide film, which acts as the dielectric, formed on the anode foil surface. A very thin oxide film formed by electrolytic oxidation (formation) offers superior dielectric constant and has rectifying properties. When in contact with an electrolyte, the oxide film possesses an excellent forward direction insulation property. Together with magnified effective surface area attained by etching the foil, a high capacitance yet small sized capacitor is available. As previously mentioned, an aluminum electrolytic capacitor is constructed by using two strips of aluminum foil (anode and cathode) with paper interleaved. This foil and paper are then wound into an element and impregnated with electrolyte.[12]

3.2.2.b) Ultra Capacitor Energy Sources (UCES):- Ultra-capacitors have distinct potential advantages for energy storage which make them almost unbeatable in many applications because they have no moving parts, and require neither cooling nor heating, and because they undergo no internal chemical changes as part of their function, they are very efficient and robust. Also, they require practically no maintenance and the lifetime is measured in decades, with no lifetime degradation due to frequent and deep cycling. They have no significant fringe fields and they are intrinsically modular which enhances reparability and allows capacity to be easily incremented. Ultra-capacitors store only a relatively modest quantity of energy, but they are capable of high power discharge rates and fast recharge.

TABLE-1

LIMITATION OF BESS, ECB AND ADVANTAGES OF UCES.

4 CONCEPT OF ESR (EQUIVALENT SERIES RESISTANCE) OF CAPACITOR

Every capacitor has some ESR. ESR is the electrical resistances in series with the capacitor plates. This includes the resistance of the metal leads and plates and the connections between them. An aluminum electrolytic capacitor has resistance in the wet electrolyte solution, and in the layer of aluminum oxide which contains high levels of water (called the "hydrated oxide"), [7]. ESR "R" is from resistance of the electrode foils, the electrolyte, the leads and each connection.[9]

Fig.1 capacitor

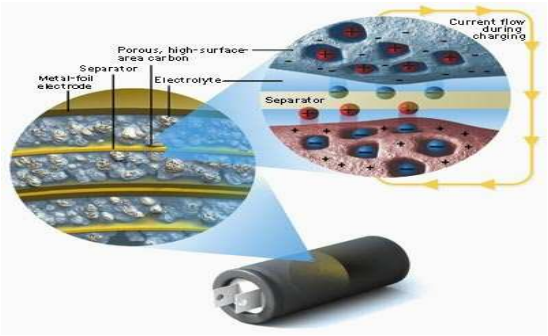

Fig.2 Ultra capacitor

5 MODELING OF ULTRA CAPACITOR

5.1 CONSTRUCTION:-The ultra-capacitor (UC) is a relative recent technology in the field of energy storage systems based on the electric double layer capacitor (EDLC or simply DLC). The construction and theory of operation of a DLC can be understood by examining the schematic view of its internal components presented. The elementary structure consists of two activated porous carbon electrodes immersed into an electrolytic solution, and a separator that prevents physical contact of the electrodes but allows ion transfer between them.

5.2 WORKING:-Energy is stored in the EDLC as a charge separation in the double layer formed at the interface between the solid electrode material surface and the liquid electrolyte in the microspores of the electrodes. This effectively creates two equivalent capacitors connected in series, which gives the name to the structure. The ultra-capacitor performance is based mainly on an

electrostatic effect, which is purely physical reversible, rather than employing faradic reactions, although includes an additional pseudo-capacitive layer contributing to the overall capacitance. Because of the complex physical phenomena in the double layer interface, traditional simple models such as the classical lumped-parameter electrical model represented by a simple RC circuit are inadequate for modeling EDLCs. Thus, this work proposes the use of an enhanced electric model of an UC based on that reflects accurately the effects of frequency, voltage and temperature in the dynamic behavior.

5.3 WORKING WITH DSTATCOM:- The model proposed, which is describes the terminal behavior of the EDLC unit over the frequency range from DC to several thousand Hertz. The VSI presented corresponds to a DC to AC switching power inverter using Insulated Gate Bipolar Transistors (IGBT). In the distribution voltage level, the switching device is generally the IGBT due to its lower switching losses and reduced size. In addition, the power rating of custom power devices is relatively low. As a result, the output voltage control of the DSTATCOM-UCES can be achieved through pulse width modulation (PWM) by using high-power fast-switched IGBTs. The terminal voltage determines the number of capacitors *Ns* which must be connected in series to form a string, and the total capacitance determines the number of capacitor strings *Np* which must be connected in parallel in the bank. The amount of energy drawn from the ultra-capacitors bank is directly proportional to the total capacitance and the change in the terminal voltage (*VUCBi*-initial and *VUCBf*-final voltages),

$$E_{UCB} = \frac{1}{2} C_{UCB} (V^2_{UCBi} \quad V^2_{UCBf}) \tag{1}$$

The integration of the UCES system into the DC bus of the DSTATCOM device requires a rapid bidirectional interface capable of both a step-down and a step-up function in the two directions (two quadrants) to obtain a suitable control performance of the overall system.[2]

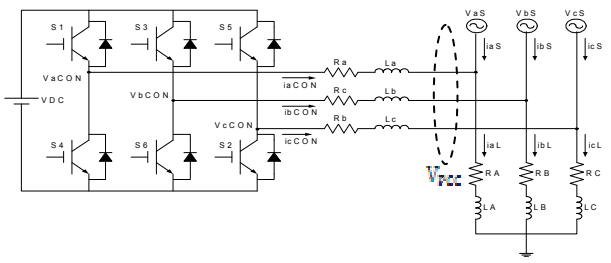

Fig. 3 Circuit diagram of DSTATCOM

6 MATHEMATICAL FORMULATION OF DSTATCOM

In steady state operation, the angle triggering angle α is very close to zero. Now, if *VPCC* < VC, reactive power flows from the DSTATCOM to the bus. So, by controlling the inverter voltage magnitude *VC*, the reactive power flow from the DSTATCOM can be regulated. This can be done in several ways. In this paper, a GTO based square wave Voltage Source Converter (VSC) is used to generate the alternating voltage from the DC bus. In this type of inverters, the fundamental component of the inverter output voltage is proportional to the DC bus voltage. So, the control objective is to regulate *VDC* as per requirement. Also, the phase angle should be maintained so that the AC generated voltage is in phase with the bus voltage.

Here, the PLL (phase lock loop) synchronizes the GTO pulses to the system voltage and generates a reference angle. This reference angle is used to calculate positive sequence component of the DSTATCOM current using a-b-c to d-q-0 transformation. The voltage regulator block calculates the difference between reference voltage and measured bus voltage and the output is passed through a PI controller to generate the reactive current reference. This reactive current reference is then passed through a current regulator block to generate the angle α. This current regulator block also consists of a PI controller to keep the angle α close to zero. The Firing Pulse Generator block generates square pulses for the inverter from the output of the PLL and the current regulator block. If due to the application of a pulsed load the bus voltage reduces to some extent, the voltage regulator changes the reactive current reference and as a result the current regulator increases the angle α so that more active power flows from bus to the DSTATCOM and energizes the capacitor. So the DC voltage increases and consequently the AC output of the inverter also increases and the necessary reactive power flows from DSTATCOM to the bus.

Active power of DSTATCOM is given as:-

$$P_{DSTATCOM} = \frac{|V_O| \cdot |V_S|}{X_T} \cdot Sin(\delta) \tag{2}$$

$$Q_{DSTATCOM} = \frac{|V_O| \cdot |V_S|}{X_T} \cdot Cos(\delta) - \frac{|V_S|^2}{X_T} \tag{3}$$

Here PDSTATCOM is the active power supply by DSTATCOM, QDSTATCOM is the reactive supply by the DSTATCOM is the output voltage of DSTACOM, V_S is the source voltage, X_T is the transformer reactance and δ is load angle. The reactive power of DSTATCOM is

When $\delta = 0$,

$$P_{DSTATCOM} = \frac{|V_O| \cdot |V_S|}{X_T} .Sin(0) = 0 \tag{4}$$

$$P_{DSTATCOM} = 0(W) \quad (5)$$

$$Q_{DSTATCOM} = \frac{|V_O|\cdot|V_S|}{X_T}\cos(0) - \frac{|V_S|^2}{X_T} = \frac{|V_O|\cdot|V_S|}{X_T} - \frac{|V_S|^2}{X_T} \quad (6)$$

$$Q_{DSTATCOM} = \frac{|V_S - V_O|V_S}{X_T} \quad [VAR] \quad (7)$$

The DSTATCOM does not supply any reactive power to the load (as shown in eq. 4) and recharge capacitor bank (as shown in eq. 6) when $\delta = 0$. When $\delta > 0$, DSTATCOM supplies the reactive power to the load. To control the reactive power flows from the DSTACOM to the load, converter's voltage magnitude V_{CON} is to be controled. Direct axis converter voltage V_{dcon} and quadrature axis converter voltage V_{qcon} is calculates as:-

$$\overline{V_{CON}} = L\frac{d\overline{i_{CON}}}{dt} + R\overline{i_{CON}} + \overline{V_S} \quad (8)$$

Where,

$\overline{V_{CON}}$ is converter voltage vector = $\begin{bmatrix} V_{aCON} \\ V_{bCON} \\ V_{cCON} \end{bmatrix}$ are converter line voltages

$\overline{i_{CON}}$ is converter current vector = $\begin{bmatrix} i_{aCON} \\ i_{bCON} \\ i_{cCON} \end{bmatrix}$ are converter line currents

$\overline{V_S}$ is the source voltage vector = $\begin{bmatrix} V_{aS} \\ V_{bS} \\ V_{cS} \end{bmatrix}$ are line voltages

Let *abc V* and 0*dq V* be voltage vectors referred to the *abc* and *0dq* reference frames, respectively. Any voltage vector in the *abc* reference can be transformed to the *0dq* reference, and vice versa [4].Neglecting zero sequence components in Park's transformation matrix given by

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t - \frac{4\pi}{3}\right) \\ \sin(\omega t) & \sin\left(\omega t - \frac{2\pi}{3}\right) & \sin\left(\omega t - \frac{4\pi}{3}\right) \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$$

[15](9)

Using Park's transformation the eq. (7) is:

$$T\overline{V_{CON}} = LT\frac{d\overline{i_{CON}}}{dt} + RT\overline{i_{CON}} + T\overline{V_S} \quad (10)$$

Now the dynamic equation governing the instantaneous values of the three-phase output voltage in the ac side of the DSTATCOM and the current exchanged with the distribution grid is given as:

$$T\begin{bmatrix} V_{aCON} \\ V_{bCON} \\ V_{cCON} \end{bmatrix} = LT\frac{d}{dt}\begin{bmatrix} i_{aCON} \\ i_{bCON} \\ i_{cCON} \end{bmatrix} + RT\begin{bmatrix} i_{aCON} \\ i_{bCON} \\ i_{cCON} \end{bmatrix} + T\begin{bmatrix} V_{aS} \\ V_{bS} \\ V_{cS} \end{bmatrix} \quad (11)$$

At any time the value of current supplied by DSTATCOM is:

$$\frac{d}{dt}(T\overline{i_{CON}}) = T\frac{d}{dt}(\overline{i_{CON}}) + \frac{d}{dt}(T)\overline{i_{CON}} \quad (12)$$

And, $T\frac{d}{dt}(\overline{i_{CON}}) = \frac{d}{dt}(T\overline{i_{CON}}) - \frac{d}{dt}(T)\overline{i_{CON}}$ (13)

The derivative of 'T' with respect to time 't' is:

$$\frac{d}{dt}(T) = \frac{2}{3}\begin{bmatrix} -\omega\sin(\omega t) & -\omega\sin\left(\omega t - \frac{2\pi}{3}\right) & -\omega\sin\left(\omega t - \frac{4\pi}{3}\right) \\ -\omega\cos(\omega t) & -\omega\cos\left(\omega t - \frac{2\pi}{3}\right) & -\omega\cos\left(\omega t - \frac{4\pi}{3}\right) \end{bmatrix} \quad (14)$$

In polar co-ordinate $\frac{d}{dt}(T)\overline{i_{CON}} = \omega\begin{bmatrix} i_{qCON} \\ -i_{dCON} \end{bmatrix}$ (15)

$$T\frac{d}{dt}(\overline{i_{CON}}) = \frac{d}{dt}\begin{bmatrix} i_{dCON} \\ i_{qCON} \end{bmatrix} - \omega\begin{bmatrix} i_{qCON} \\ -i_{dCON} \end{bmatrix} \quad (16)$$

So eq. (1) in d-q form is:

$$\begin{bmatrix} V_{dCON} \\ V_{qCON} \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_{dCON} \\ i_{qCON} \end{bmatrix} + R\begin{bmatrix} i_{dCON} \\ i_{qCON} \end{bmatrix} + \begin{bmatrix} V_{dS} \\ V_{qS} \end{bmatrix} - \omega L\begin{bmatrix} i_{qCON} \\ -i_{dCON} \end{bmatrix} \quad (17)$$

From eq. (10) the direct axis and quadrature axis voltage is define as:

$$V_{dCON} = L\frac{d}{dt}(i_{dCON}) + Ri_{dCON} + V_{dS} - \omega L i_{qCON} \quad (18)$$

$$V_{qCON} = L\frac{d}{dt}(i_{qCON}) + Ri_{qCON} + V_{qS} + \omega L i_{dCON} \quad (19)$$

By taking $V_{dS} = V_S$ and $V_{qS} = 0$, direct axis and quadrature axis voltage is:

$$V_{dCON} = L\frac{d}{dt}(i_{dCON}) + Ri_{dCON} + v_S - \omega L i_{qCON} \quad (20)$$

$$V_{qCON} = L\frac{d}{dt}(i_{qCON}) + Ri_{qCON} + 0 + \omega L i_{dCON} \quad (21)$$

ωLi_{qcon} and ωLi_{dcon} have very small value, so can be neglected. Solving with help of Laplace transformation of eq. (13) and (14)

$$V_{dcon} = sLI_{dcon} + RI_{dcon} \quad (22)$$

$$V_{qcon} = sLI_{qcon} + RI_{qcon} \quad (23).[3]$$

7 SIMULATION RESULTS AND DISCUSSION

7.1 WITH ELETOLYTIC CAPACITOR BANK:- Electrolytic Capacitor 470µf, 450V, with series parallel combination ESR=9.8mΩ,total resistance with balance resistance 5Ω, Kemet electrolytic Capacitors.[8]

7.2 SIMULATION WITH ULTRA CAPACITOR: - A DSTATCOM connected with ultra capacitor of voltage 2.7V,capacitance 650f and ESR =0.80mΩ. [9]
Figure 1 to 5 shows operation of ULTRA CAPACITOR with DSTATCOM. The ultra capacitor has very low degradation after 100000 cycle of charging and discharging.

COMPA,RISON BETWEEN ELECTROLYTIC AND ULTRA CAPACITOR

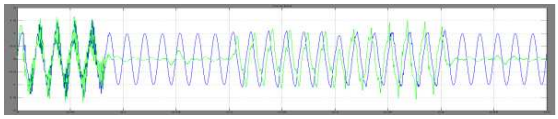

fig. 4(a)

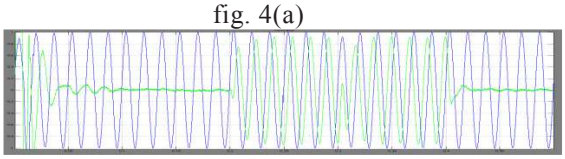

fig. 4(b)

The current and voltage in per unit is shows in fig. 4(a) with electrolytic capacitor and 4(b) with ultra capacitor.

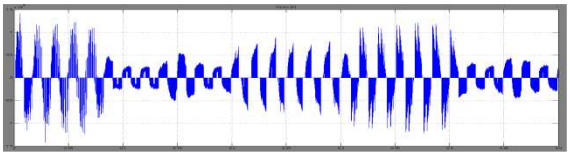

fig. 5(a)

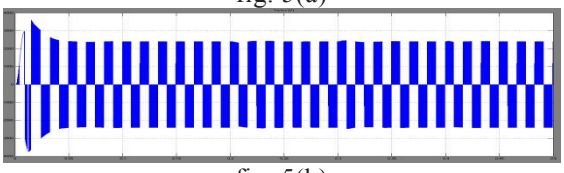

fig. 5(b)

The voltage across the converters is shows in fig. 5(a) with electrolytic capacitor and 5(b) with ultra capacitor.
The variable load produces the voltage dip from 0.2 to 0.3 sec. The voltage and current measurement (on BSTATCOM) measure the voltage and current on 0.2 sec. When the voltage dip is sensed by voltage controller, it sends the signal to PWM signal generator. The PWM signal generator operates the IGBTs. The energy of capacitor bank supplies to the load via IGBTs. The voltage is controlled by injecting the current in line by DSTATCOM. By equation number (8) the direct axis and quadrature axis voltage is changed into three phase voltage and three phase voltage is change into direct axis and quadrature axis voltage using Park's transformation. Current also follows the same Park's transformation. Due to balancing resistances used in electrolytic capacitor bank, the output wave is not pure sine wave, it is distorted. The voltage across the inverter is not uniform as in the fig. 4(a). During test load condition from 0.2 to 0.3sec the voltage across the inverter circuit is more than with ultra capacitor. When the load changes from inductive to capacitive during 0.3 to 0.4 sec the voltage across inverter circuit is reaches 10 kv, which is too high.

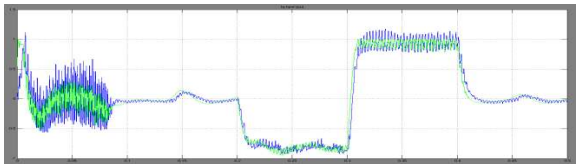

Fig.6(a)

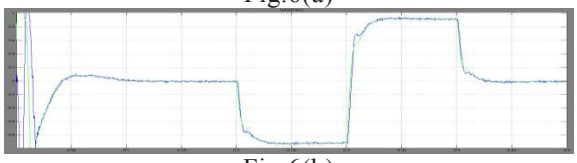

Fig.6(b)

The quadrature axis current Iq and quadrature axis reference current Iqref Fig.6(a) with electrolytic capacitor and 6(b) with ultra capacitor.

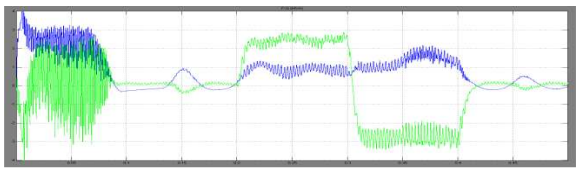

fig. 7(a)

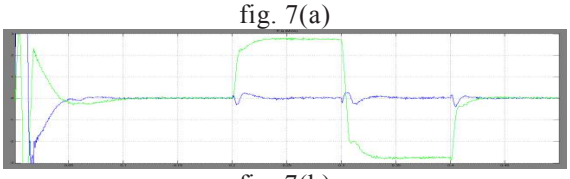

fig. 7(b)

Active and reactive power supply by DSTATCOM, fig. 7(a) with electrolytic capacitor and 7(b) with ultra capacitor.
The inductive load is switched on, on 0.2 sec. On that time current injected by capacitor bank (electrolytic type) produces harmonics which causes the distorted wave form of 7(a) and 7(b). But when use ultra capacitor bank, the harmonics are reduces and quadrature axis current is less distorted.

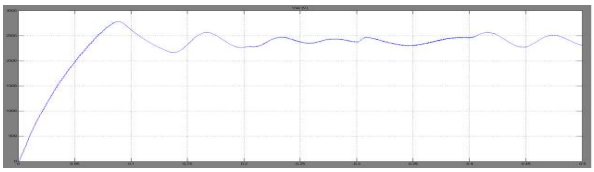

fig. 8(a)

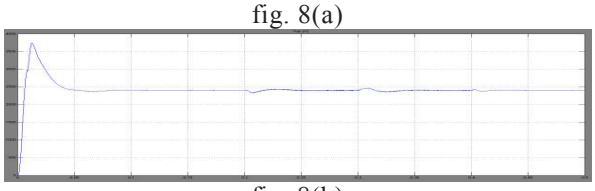

fig. 8(b)

DC bus voltage, fig. 8(a) with electrolytic capacitor and 8(b) with ultra capacitor.

Dc bus voltage reduces on same power output of DSTATCOM because of less harmonics produce by ultra capacitor.

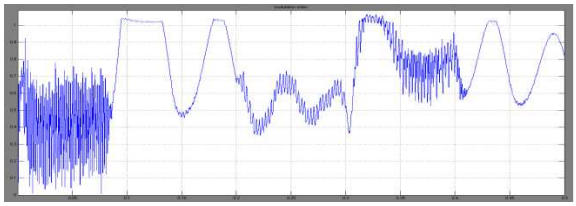

fig. 9(a)

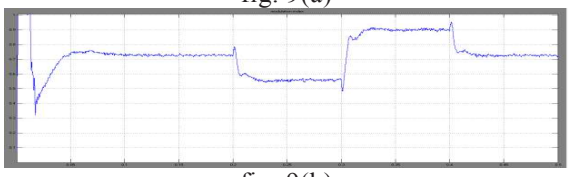

fig. 9(b)

Modulation index, fig. 9(a) with electrolytic capacitor and 9(b) with ultra capacitor.

Inductive and capacitive load handling capability is improve as shown in fig 4(a). From equation (1) and (2), the energy supplied by capacitor bank is given by P,Q plot, current injected is given by Iq graph, voltage across capacitor bank is given by DC bus voltage and modulation index shows the DSTATCOM operation with inductive and capacitive load.

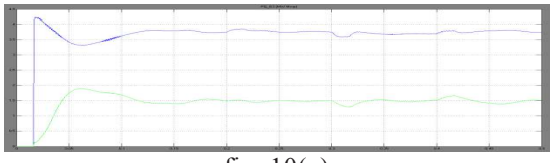

fig. 10(a)

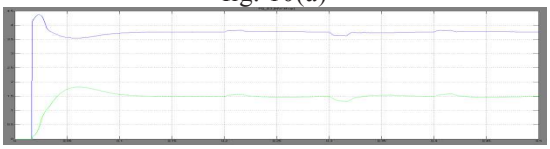

fig. 10(b)

The active and reactive power supply on bus B3, 10(a) with electrolytic capacitor and 10(b) with ultra capacitor.

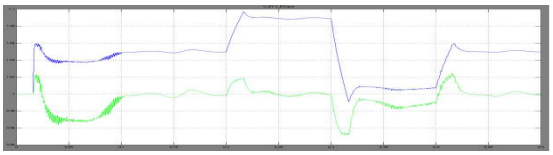

fig. 11(a)

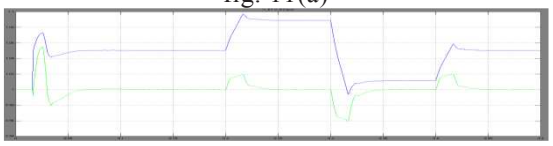

fig. 11(b)

The voltage across bus B1 and B3 in per unit, fig. 11(a) with electrolytic capacitor and 11(b) with ultra capacitor.

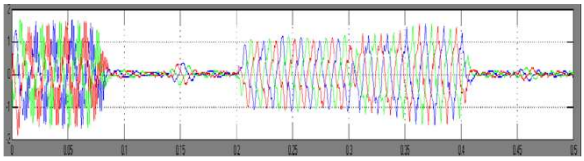

fig. 12(a)

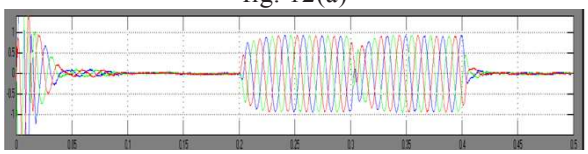

fig. 12(b)

The three phase current injected by DSTATCOM, fig. 12(a) with electrolytic capacitor and 12(b) with ultra capacitor.

The load is change from inductive to capacitive from 0.3 to 0.4 sec. On sec 0.3, controller operates to change conduction angle of IGBTs and capacitor bank. The active and reactive power shows in fig. 7(a). Small dip in graph on 0.2 sec is due to load applied is inductive, and dip on 0.3 sec is due to load change from inductive to capacitive. Bus B3 is near the load and having more voltage because reactive power is supplies through it but Bus B1 is not much affected by that as in fig. 7(b). Fig. 8(a) shows the converter current in per unit. The electrolytic type capacitor bank have the more distortion than ultra capacitor because of more charging and discharging time. During capacitive and inductive load, the three phase current injected by the DSTATCOM is shown Fig.8(b).

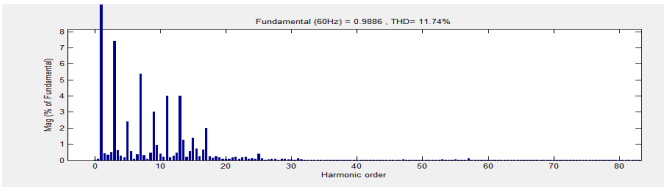

fig. 13(a)

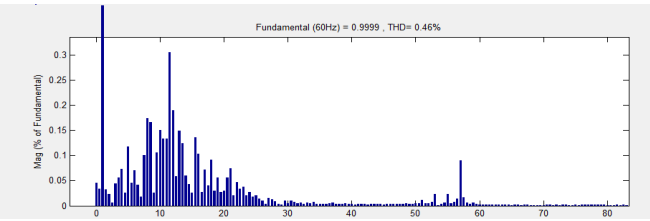

fig. 13(b)

Voltage harmonics produce by DSTATCOM on 0.35 sec. fig. 13(a) with electrolytic capacitor and 13(b) with ultra capacitor.

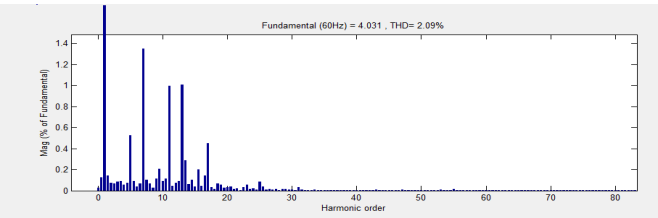

fig. 14(a)

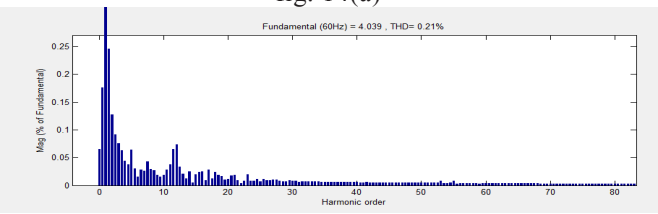

fig. 14(b)

Current harmonics produce by DSTATCOM on 0.35 sec. 15(a) with electrolytic capacitor and 15(b) with ultra capacitor.The harmonics produces by a DSTATCOM must be as IEEE standard. The inductive load is connected to distribution line on 0.2 sec. the load is change from inductive to capacitive on 0.3 sec. on that time the capacitor bank also having capacitive energy, so on time 0.35 sec and 2 complete cycle of voltage and current wave, the harmonics are maximum. But when we compare the harmonics produces by DSTATCOM with electrolytic and ultra capacitor bank, the result are much better with ultra capacitor.

8 CONCLUSION

By use of UCES in DSTATCOM gives ultra fast response to voltage sag and swell. For economical aspects the UCES is prefer over electrolytic type capacitor bank because of long life and less harmonics.

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